Scaling Effectiveness of the Existing Research Techniques towards improving problems in Reversible Logic

Nayana D.K
Research Scholar
Jain University
Bangalore, India
Email: - nayanadk08@gmail.com

Sujatha B.K
Prof., Dept. of Telecommunication Engg. MSRIT,
Bangalore, India

Abstract— Till date, majority of the hardwares of the computing devices are found to use irreversible logic that works on the principle of elimination of bits of data. Such technique increases exponential thermal dissipation causing degradation in the performance of the controller or the computing devices. The solution to this technique is usage of reversible logic that tremendously reduces the thermal dissipation and explores its usability in the low-powered computing devices. However, accomplishment of complete reversibility is still an open-end question but some amount of research initiative already started in recent times. Inspite of less availability of standard implementation works towards reversible logic, the prime contribution of this paper is to discuss the essentials of it followed by explicit discussion of advantages and pitfalls of existing research approaches towards enhancing reversible logic. The paper also discusses about the research gap that is extracted after reviewing the effectiveness in this perspective implementation.

Keywords- Irreversible, Reversible Logic, Thermal Dissipation, Logic Gates, Logic Performance.

I. INTRODUCTION

With the radical changes introduced by VLSI (Very Large Scale Integration), there has been evolution of miniaturization of various electrical and electronic components. It has not only lowered the sizes of the controllers but also successfully introduced many novel features to welcome the technological advancement. This is only possible when more number of logical elements in minimal volumes are used with maximized clock frequencies are used. Unfortunately, it gives rise to three issues i.e. i) faster drainage of battery life, ii) financial loss due to energy loss, and iii) overheating of the system thereby degrading their performance. In order to eliminate a bit of data, a computational system will need to spend a significant amount of energy (2kT, where k=Boltzmann's constant and T is room temperature) [1]. At present a single logical operation will lead the computer to eliminate a bit of data all the time around and such mechanism is called as irreversible [2]. The drawback of this irreversible technique is its inefficient elimination process and increasing dependencies to expend more thermal coefficient (even more then kT) in real time [3]. Hence, such deployment of irreversible process in circuit design is definitely not recommended as the power consumption is increasingly high. Therefore, in order to enhance the hardware component of the computing device, it is necessary to address the problems of energy dissipation owing to the usage of irreversible logic. At present, there is a technique that performs improvement on the top of irreversible logic while on the other hand there is evolution of reversible logic-based circuits. From the theoretical viewpoint, introduction of reversible logic is meant to cater up the defects of the conventional irreversible logic-based circuit in perspective of power consumption. Usages of reversible logic ensure zero elimination of the bits of data by its logical operation [4] although they too dissipate certain smaller quantity of heat in preliminary stages of operation. At present, there are certain degrees of initiatives among the researchers to work in reversible logic. There are less than 40 research journals published during 2010-2016 pertaining to reversible logic in IEEE Xplore. This figure itself shows that there are very less implementation work done towards reversible logic.

Hence, this paper discusses about the effectiveness of all the available significant research journals. Sub-Section a discusses about the background of the study mainly highlighting the frequently used techniques followed by problems identification in Sub-Section b and proposed system in Sub-Section c. Section II discusses about existing research trends toward reversible logic followed by brief description f research gap in Section III and conclusion in Section IV.

A. Background

This section discusses about background of the existing research techniques implemented towards improving the

performance and implementation feasibilities of reversible logic. Some of the standard research techniques are as follows:

- *Decomposition Techniques:* There are various decomposition-based scheme that splits the main function for subjecting it to realization of a discreet reversible network. Existing techniques of decomposition includes-decomposition, analysis of modified reconstruct ability, Ashenhurst-Curtis decomposition [5].
- *Genetic Algorithm:* This is mainly used for search optimization using evolutionary technique. This technique is found to be highly suitable for reducing the effect of partial functions specified. Usage of genetic algorithm is quite essential for realizing the minimal forms of function with an aid of structures of reversible forms [6].
- *Composition Techniques:* These types of techniques make use of very less and frequently deployed reversible gates while developing blocks of reversible circuits. A traditional synthesis process is applied for synthesizing the core networks [7].
- *EXOR Techniques:* This is another frequently used technique that is also associated with the deployment of Toffoli gate. Such techniques are normally used by Toffoli gate for performing heuristic-based synthesis [8].
- *Hypothetical Grouping Techniques:* Grouping technique is another standard technique used in designing logical circuits. The serial-based connectivity as well as parallel-based connectivity is set using representation form of k-cycle of grouping. Various permuting steps are undertaken on smaller steps while designing reversible circuits. However, this technique is highly dependent on its specification [9].
- *Search-based Techniques:* The prime goal of any design principle of circuit is to ensured uniform functionality of output irrespective of any expansion or reduction in the circuitry components. This process yields better compactness in the circuit design after particular operational rounds. The prime pitfall of this technique is its nature of expensive implementation scheme owing to increasing needs of spacing in circuitry design with progress in search [10].

B. The Problem

At present, the prime problem identification in design principle of VLSI is question of reliability as well as trustworthy in terms of highly minimal power consumption. Such need of low power consumption is the only source of reliability during processing (followed by transmission) of the signals in order to sustain higher degree of integrity. At present, the design principle of the circuits in the controller is not deployed with reversible logic that causes extensive thermal dissipation leading to progressive power consumption. Such problems can be significantly controlled by using devices equipped with reversible logic. According to the fundamental of reversible logic implementation, it is said not to develop much output of sub-circuits and gates as such they will be required to be deployed as input for other gates too as a part of reversibile logic. This is the prime reason that posses a challenge to develop an effective synthesis technique for reducing the garbage signals cardinality. It is also essential to maintain lower number of constants at the input gate while developing the reversible circuits. Hence, if there is any form of dependencies towards using replicas of signal that conventional Feynman gate can be deployed. It is also essential that the resulting circuit should be free from any loops. The technique doesn't allow fan-out operation and hence the realization of the reversible logic can be carried out by inversing the specification of gates in opposite order. However, such process is not that simple and still need more ground-breaking research to overcome various unsolved problems.

C. The Proposed Solution

The prime aim of this paper is to highlight the effectiveness of the usage of reversible logic in the circuit design. Although, there are discussion papers present but less number of research paper exist that has measured the effectiveness of existing reversible logic-based circuits. Hence, this paper aims to discuss the benefits as well as pitfalls of various research work towards reversible logic to understand the problems that has not been attended much by the existing researchers. The next section discusses about the essential information of reversible logic.

II. ESSENTIALS OF REVERSIBLE LOGIC

The significance of the reversible computing is quite high in upcoming future where various types of miniature-based applications will be evolved. Such forms of application will be sustained by low-powered supply of energy. It is more likely that reversible computing and its usage will become more prevalent as this technology ensures lowered consumption of power. A circuit designed by reversible logic will always have equivalent number of inputs and outputs. They will also have one-to-one mapping relationship among the communication vectors of both input as well as output. Therefore, it is feasible to construct the input state vector to be generated from the output state vector. A communication is supposed to be a reversible in nature if it is feasible to specifically extract the input for a given output. This technology permits to design and develop a reversible gate by appending certain extra input and output wires on demand. From the mathematical viewpoint, a function g(x) where x=x1, x2, ….., xp can be called as reversible function if it satisfies the two conditions i.e. i) the output cardinality should be equivalent to that of inputs and ii) a pattern of any input should map with particular pattern of output. For a (p, q) based function (means p-inputs and q-outputs), it is required that certain output and / or input should be appended in order to convert it into reversible. The inputs

that are constant are also termed as ancilla input. The basic structure of reversible circuit is as follows:

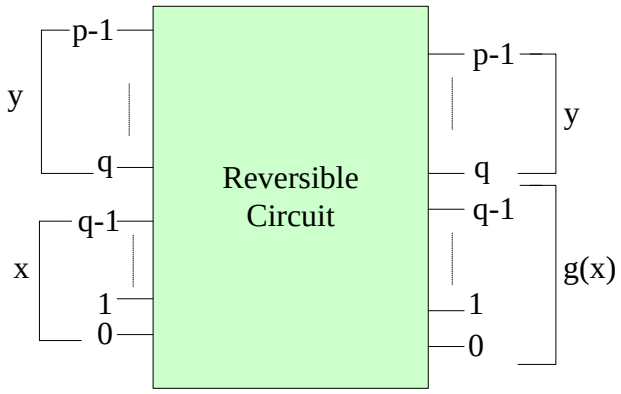

Fig.1. Example of Reversible Circuit

It is basically the cardinality of output that is also known as garbage that is responsible for rendering the function reversible. Basically, the uniform inputs and the garbage outputs are also empirically shown as,

Constant input+input=garbage+output

Hence, a reversible gate is believed to posses a reversible circuit with equivalent number of output and input wires. Empirically, a reversible circuit is expressed as p x p circuit where p is the number of inputs. The fig.1 shows a normal reversible circuit where the upper p-q lines transfer p-q signals to the wires that correspond to the other circuits on other sides. The lower q wires is considered to be input for X and evolve out as output corresponding to the value of g(X). Such wires are often considered to be served as workspace in order to compute the reversible function. Therefore, in order to accomplish reversibility, there is a need for both functional outputs and garbage outputs. Some of the frequently used gates in reversible logic are i) Toffoli gate, ii) Feynman gate, and iii) Fredkin gate. The brief descriptions of them are as follows:

- *Toffoli gate* [11]: This type of gate is basically known as universal logic gate that is capable of constructing any reversible circuit. Fig.2 show Toffoli gate with 3-bit input as well as output where it starts inverting after setting the initial two bits. Otherwise, all the presented bits don't alter. It is also called as controller-controller-not gate or 3*3 Feynman gate very frequently.

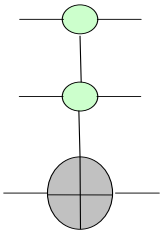

Fig.2. Toffoli Gate

- *Feynman gate* [12]: Basically, a Feynman gate has 2x2 gate. Fig.3 shows the normal Feynman gate with inputs A and B, whereas the outputs are P and Q, where P is equivalent to A and Q is XOR of both the inputs A and B. Feynman gate is considered to have quantum cost of unity. The application of this gate is more towards replicating outputs in the gate.

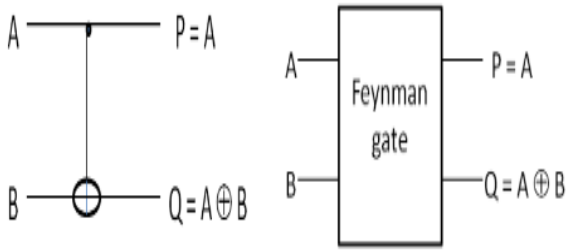

Fig.3. Feynman Gate

- *Fredkin gate* [13]: This is another frequently used gate in designing circuits with universal reversible logic. Using Fredkin gates allows applying various forms of arithmetic as well as logical operation. Fig. 4 highlights the normal Fredkin gates that shows 3*3 gate configuration with three different types of inputs A, B, and C and the output of P, Q, and R. According to the definition of Fredkin gates, the output vector P is equivalent to A, Q is equivalent to XOR of A'B and AC, while R is equivalent to XOR of A'C and AB.

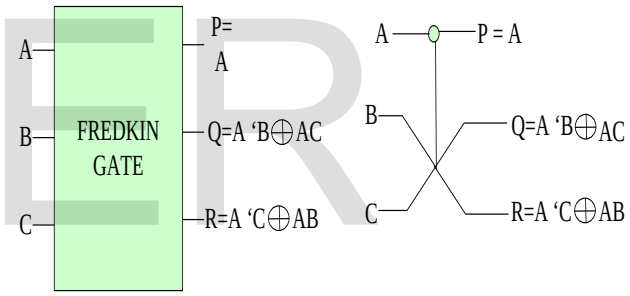

Fig.4. Fredkin Gate

Apart from the above mentioned gates, the other forms of gates are Peres gates [14], TSG gate [15], Sayem gate [16], and D-latch [17]. Another most significant process in reversible logic is to eliminate the garbage output in order to resist the loss of energy owing to aggregation of garbage output. IN such condition, the circuits are inversely constructed.

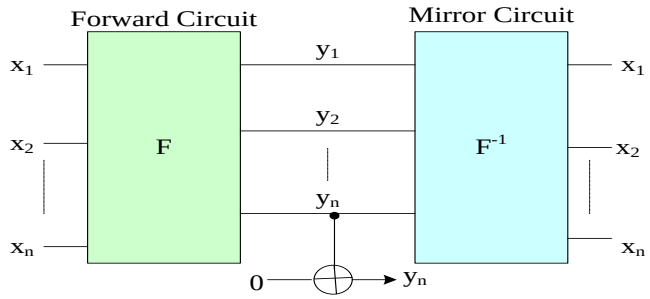

Fig.5. Process of garbage elimination

Fig.5 shows the process of garbage elimination where the inverse operation is carried out by considering the outputs of

the reversible circuits and subjecting it to inverse of the input signals. This phenomenon is quite essential when it comes to quantum computing [18] that doesn't permit any possible operations of the garbage. The above figure exhibits a forward and mirror circuit which is just the opposite of inverse operation. A reversible function is realized only on such gates. Therefore computing the inverse function for any output vector is nearly equivalent to transmitting the similar pattern in reverse direction using the same circuits. The next section discusses about the exitsing research contribution in the same field.

III. RESEARCH CONTRIBUTION TOWARDS REVERSIBLE LOGIC

This section discusses about the significant work being carried out towards mechanizing an improvement in research work towards Reversible Logic (RL). Although, there are various review papers being present over internet sources, there is so significant journal pertaining to review work about the topic present in reputed publishers in IEEE, Springer, Elsevier, etc. Hence, in order to maintain reliability and standard, we do not consider discussing any papers from other sources apart from the most standard publishers. The research contribution discussion in this section is published between the years 2010-2016.

The most recent study of reversible logic has been carried out by Bolhassani and Haghparast [19] where the authors have optimized various components of reversible logic using hardware-based approach. Kalita and Saikia [20] have presented a technique by implementing various mathematical and logical operations for enhancing the base operation of reversible logic as well as quantum logic. Jayashree et al. [21] have presented a design of reversible logic by implementing an integer multiplier. The work has been carried out by enhancing the traditional adder and shift technique to find approximately 90% enhancement with respect to ancilla qubits as compared to existing system. Enhancement towards multiplier operation was also emphasized by Rajmohan and Maheshwari [22] in their work where a 5x5 multiple cell was introduced. The author claimed that the technique is capable of retaining regularity among the array multipliers. Tabatabaii et al. [23] have emphasized on fault tolerance associated with floating point addition. The authors provide the solution by introducing reversible floating point adder for parity preservation. The technique also uses scale of nanometer. Similar type of work has also been carried out by Gaur and Singh [24] for generating reversible circuits to preserve parity. Tofolli gates have been presented using multiple controlling approaches and were implemented over benchmarked circuits. Bahar et al. [25] have implemented cellular automata concept that suits well with nano technology with quantum dots approach. The study outcome was found to show 233 times reducting in layout size as compared to any conventional CMOS technology. Sarker et al. [26] have developed a new design of ALU that has the capability of carrying out 3 arithmatic operation and 4 logical operations using DNA-based multiplexer design.

Datta et al. [27] have emphasized on optimizing tofolli gates with negative control. The technique also emphasizes working on both positive as well as negative control lines using recursive approach of merging and substitution rules. Khan et al. [28] have presented a technique that introduces sequential cirucits with an effective synchronocity for enhancing the operation of the reversible logic. The technique was also found to use Reed Muller approach where the study outcome was found to achieve approximately 49% of saving of quantum cost and 81% of garbage outcome compared to designs of existing system. Sethi and Roy [29] have used gates with reversible logic applicable in optical network. The technique was implemented over a resonator of 2x2 add-drop microring using Toffoli logic fates with 85% of maximized modulation depth. Babu et al. [30] have introduced an algorithm for the purpose of optimizing comparator by incorporating two types of gates. The study outcome was witnessed to find significant outcomes with respect to quantum cost, garbage outputs, number of gates, and minimization of the area. Thapliyal et al. [31] have presented a work for developing a test framework for evaluating reversible logic. The technique includes developing dual vectors on conservative logic gates which sequential circuits were introduced over the conventional gate system in order to performing testing. The technique also uses latches for testing, flip flop operation with master and slave configuration, as well as flip flop operation with double edge triggered approach. The study outcome was found to offer full fledge fault tolerance for any forms of defects in cellular automata.

Li et al. [32] have presented a study towards formulating computational algorithm for enhancing the RL operation of 4 bits. The authors have used hash table over 3 bit synthesis algorithm for the purpose of optimizing 4 bit RL. Sen et al. [33] have addressed the problem of the fault tolerant for RL based circuits. The authors have presented the design of reversible adders using cellular automata where the study outcome was claimed to offer approximately 47% of efficiency in presence of cell defects. Thomsen [34] have presented an optimization technique for improving RL circuits. The mechanism of solution was based on functional language. A unique study was presented by Dreshsler et al. [35] by introducing evolutionary algorithms as a mean to optimize the RL based circuits. The technique was found to offer better circuit realization using less operational cost. Roy et al. [36] have used multiple types of gates in order to control microresonators using hardware-based approach. Mahammad and Veezhinathan [37] have designed and implemented universal RL gate that can be used similar to the operation carried out by lookup table in FPGA. Thapliyal et al. [38] have presented a technique that uses analysis of the patterns of the faults in highly conservative way. Various testable latches were used for this purpose mainly using the Fredkin gate. The technique is meant for evaluating both permanent and temporary faults. The study outcomes was tested using verification of the latches using number of clock cycles as well as number of gates used in the system over different lock configurations. The summary of all these existing technqiues has been tabulated below in Table 1.

Table.1. Summary of Existing Research Contribution

Author	Problem Addressed	Technique Applied	Remarks
Bolhassani [19]	Design optimization of RL	3x3, 4x4 RL blocks	Pros: Addressed hardware complexity Cons: Doesn't address power analysis
Kalita [20]	Implementing Quantum logic	Quantum Logic, micro-operations	Pros: Simpler implementation Cons: No comparative analysis, lesser optimization of quantum cost
Jayashree et al. [21]	Quantum operation	Optimizing conventional adder and shift	Pros: 90% improvement in ancilla qubits. Cons: Doesn't focus on overall circuit optimization
Rajmohan [22]	Enhancing multiplier operation	5x5 reversible multiplier cell	Pros: Enhance multiplication and adding operation Cons: Narrowed Study scope on large circuits
Tabatabaii et al. [23]	Complexity of floating point addition	reversible floating point adder	Pros: Works on naometric scale Cons: No benchmarking
Gaur [24]	Parity preserving	Tofolli gates	Pros: 32% minimization of operating cost Cons: Doesn't focus on overall hardware complexity.
Sarker et al. [26]	Realization of ALU	DNA-based multiplexer	Pros: Minimize complexity. Cons: No focus on division operation
Datta et al. [27]	Enhancement of Tofolli gates	Optimization (post synthesis)	Pros: reduces number of gates, minimize quantum cost Cons: Didn't address space complexity
Khan et al. [28]	Lowering quantum cost in RL design	Reed Muller, sequential circuits	Pros: Minimization of quantum cost Cons: No focus on power performance.
Sethi [29]	Reconfigurability in optical network	Toffoli gates, switching with free carrier injection	Pros: Good Theoritical modeling Cons: No comparative analysis
Babu et al. [30]	Optimization of the comparator	Incorporation of gates (i) Hasan-Lafifa-Nazir gate, ii) Babu-Jamal-Saleheen gates)	Pros: Significant improvement in area and number of gates Cons: Lower quantum cost
Thapliyal [31], Mahammad [37]	To develop testable circuits using RL	Flip-flop based test modeling	Pros: Exhibt better performance Cons:No significant extensive / comparative analysis
Li et al. [32]	4bit RL circuit	Hash table, NOT gate, Controlled gate, Toffoli gate	Pros: Good algorithmic description. Cons: No significant extensive / comparative analysis
Sen et al. [33]	Fault Tolerance	Reversible adders	Pros: Addresses design and cost complexity Cons: No comparative study.
Dreshsler et al. [35]	Enhancing RL circuits	Evolutionary technique	Pros: less cost Cons: No comparative study
Roy et al. [36]	Enhancing RL gates	Reversible gates of all optics	Pros: Applicable on large circuits

			Cons: No comparative study

IV. RESEASRCH GAP

After reviewing the existing research contribution towards reversible logic, it has been found that all the existing techniques are associated with certain advantages as well as limitations too. Although, every research work has some defined set of limitation, but we will like to look into the problematic factors that were left unattended by the researchers in existing system. Hence, the problems that have been left unexplored in the existing research contribution are:

- *Less Emphasis on Power Factor:* Although, it is already known that reversible logic is made only to ensure that it provide power efficient circuit design, but various existing authors have presented this in various forms (especially by controlling the number of components involved in arithmetical and logical operation). There are few studies which has considered power as performance factor and yet there is no such discussion of any optimization techniques that has proved energy efficiency either numerically or graphically.
- *Less Comparative Analysis:* The existing research work has exhibited its outcome with respect to its own performance parameters e.g. operating cost, fault tolerant, etc. The outcomes are less found to be compared with other similar forms of techniques. Due to this lack of comparative analysis, it is quite difficult to understand the uniqueness and extent of effectiveness in the presented study.
- *Less Work towards Large Scale Deployment:* The most frequently used Fredkin and Toffoli gates are used for overcoming the thermal waste associated with the computation where bits vanished into heat and there is no energy input required to perform computation. One of the obvious problem in implementing reversible gates is that original energy preservation factor is directly proportional to the extent of slowliness of operating such gates. Moreover, it is also required for a reversible circuite to posse's adiabatic characteristic in order to retain maximum equilibrium everytime. But there are less focus of work in such direction when considering a larger scale of deployment.

V. CONCLUSION

This paper has mainly discussed about the essential of the reversible logic by stating that existing mechanism uses irreversible logic which is highly detrimental for hardware performance. Reversible logic doesn't work on the principle of bit elimination process but ensure that there is lesser energy dissipation. As the topic is quite new, so we find that there are very less numbers of research journals pertaining to improvement of reversible logic. Hence, we reviewed almost all the significant research journals published during 2010-2016 about reversible logic and highlight its advantages along with pitfalls. Finally, the review also briefs about unsolved problems in this perspective as research gap. Overall, we found that problems of energy dissipation is still unsolved and hence or future work will be in similar direction.

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